AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (currently amended) A circuit to drive a high-voltage H-bridge using CMOS technology comprising:

a control logic circuit having ~~an~~ inputs and ~~an~~ output, wherein ~~the~~a first input is a signal defining the direction of the current between the mid-points of the H-bridge and a second input comprises control signals defining the behavior of said H-bridge and the output are control signals for the high-side and low-side drivers of said H-bridge;

a power management module having an input and ~~an~~ outputs wherein the input is a battery voltage and a first~~the~~ output is a voltage to feed the low-side drivers and a second output feeds a ~~means to drive at the battery voltage level~~;

said charge pump~~means to drive at the battery voltage level~~ to drive the high-side drivers of the H-bridge and to drive a means for reverse supply protection, wherein said charge pump comprises a switching network controlled by a clocking scheme;

said means for reverse supply protection;

said two high-side drivers of the H-bridge having ~~an~~ inputs and an output, wherein ~~the~~a first input are said output control signals from said control logic circuit and a second input is a voltage from said charge pump~~charge pump~~ and

eachthe output is driving one of twothe high-side transistors of said H-bridge via a resistor each;

a first two voltage dividers, wherein a first resistor is coupled between the output of the first of said two high-side drivers and a first midpoint of said H-bridge and a second resistor is coupled between said first midpoint and ground voltage, keeping the reference voltage of said first high-side drivers on the voltage levels of thesaid first midpoints of said H-bridge;

a second voltage divider, wherein a first resistor is coupled between the output of the second of said two high-side drivers and a second midpoint of said H-bridge and a second resistor is coupled between said second midpoint and ground voltage, keeping the reference voltage of said second high-side driver on the voltage level of said second midpoint of said H-bridge;

said two low-side drivers having an input and an output, wherein thea first input input are said output control signals from said control logic circuit and a second input is the first output voltage from of said power management module and eachthe output is driving one of twothe correspondent low-side transistors of said H-bridge;

said two high-side transistors of said H-bridge being connected between the battery voltage and the midpoints of said H-bridge having each itstheir gates connected to the output of one of said two related high-side drivers via one of said resistors each;

said two low-side transistors of said H-bridge being connected between the mid-points of said H-bridge and ground having their gates connected to the output of one of said related lowhigh-side drivers; and

a load between the midpoints of said H-bridge.

2. (currently amended) The circuit of claim **1** wherein said control logic circuit, said power management module, the switching part of said means to increase battery voltage, said two high-side drivers, said voltage dividers, and said low-side drivers are all implemented on one ASIC.

Claims 3-5 (canceled)

6. (currently amended) The circuit of claim **1** wherein said module for reverse supply protection and said high-side and low-side transistors are implemented outside of an ASIC.

Claims 7-8 (canceled)

9. (currently amended): The circuit of claim ~~8~~**1** wherein said clocking scheme is a two-phase clocking scheme.

10. (currently amended): The circuit of claim ~~7~~**1** wherein said charge pump comprises two external capacitors.

11. (original): The circuit of claim **10** wherein said two external capacitors are ceramic capacitors.

12. (currently amended): The circuit of claim **1** wherein said module~~means~~ for ~~external~~ reverse supply protection is driving a transistor to inhibit any reverse supply situation.

13. (original): The circuit of claim **12** wherein said transistor is a N-channel MOS power transistor.

14. (original)The circuit of claim **1** wherein said two high-side transistors are N-channel MOS power transistors.

15. (original) The circuit of claim **1** wherein said two low-side transistors are N-channel MOS power transistors.

16. (original) The circuit of claim **1** wherein the load of said H-bridge is controlled by signals using pulse width modulation (PWM).

17. (original): The circuit of claim **1** wherein said load between the midpoints of said H-bridge is a DC-motor.

18. (original) The circuit of claim **17** wherein the direction of the rotation of said DC-motor is controlled by a direction bit.

19. (original) The circuit of claim **17** wherein the velocity of said DC motor is

controlled by signals using pulse width modulation (PWM).

Claims 20 – 21 (canceled)

22. (original)The circuit of claim **1** wherein said high-side drivers and said low said drivers work in a push-pull configuration.

23. (original): The circuit of claim **1** wherein each of said high-drivers comprises:

a semiconductor switch;

an analog controller having an input and an output, wherein the input are pulses defining the cycles of said semiconductor switch and the output are currents to control said switch; and

a means to provide a bias voltage to said semiconductor switch.

24. (original): The circuit of claim **23** wherein said semiconductor switch is a CMOS FET.

25. (original): The circuit of claim **23** wherein said means to provide a bias voltage is a resistor.

Claims 26-44 (canceled)